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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,054	10/15/2003	Jim Wang	CE11290JI290	7195

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EXAMINER	
LO, SUZANNE	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

Office Action Summary	**Application No.** 10/686,054	**Applicant(s)** WANG ET AL.	
	Examiner Suzanne Lo	**Art Unit** 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been presented for examination.

Claim Rejections - 35 USC § 101

2. Claims 1-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, claims 1-19 do not produce a tangible result. In claim 1 the final result of the method of performing PCB panel optimization is "adjusting an array layout and selecting an optimum panel dimension". Given the broadest reasonable interpretation, the final result of the method is not in a tangible form. The "adjustment" of an array layout may only be a modification of an array layout model as the specification of the instant application gives no indication that an actual physical array layout is adjusted. Additionally, the "selection" of the optimum panel dimension does not require a real world result but rather, only a logic process that exists in the abstract. Similarly, the "fitting the PCBS onto the at least one array" of claim 12 may only be a modification of a PCB panel model as the specification gives no indication that actual physical PCBs are fitted into a PCB panel.

Claim Rejections - 35 USC § 103

3. Claims 1-3, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Young et al. ("Handling Soft Modules in General Nonslicing Floorplan Using Lagrangian Relaxation") in view of Chen et al. ("Floorplan Sizing by Linear Programming Approximation").**

As per claim 1, Young is directed to a method for performing Printed Circuit Board (PCB) panel optimization, comprising the steps of: performing a panel dimension loop that goes through a plurality of possible panel dimensions **(page 690, Section C, Algorithm Solve-LDP)**; performing an array length loop that goes through a plurality of array lengths **(page 690, Section B, Algorithm Find-Width)**; performing an array width loop that goes through a plurality of array widths **(page 690, Section B, Algorithm Find-Width)** but fails to disclose calculating a panel efficiency factor for each iteration of each of the loops *and adjusting an array layout and selecting an optimum panel dimension for the PCB panel based on optimum calculated panel efficiency.*

Chen teaches calculating a cost function **(page 470, Section 4.2 "Cost Function Approximation")** *and adjusting an array layout and selecting an optimum panel dimension for the PCB panel based on optimum calculated panel efficiency* **(page 469, Section 3.1, "Area Constraint Approximation" and Section 4, "Finding the Optimum Solution").** Young and Chen are analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young with the efficiency factor calculation method of Chen in order to find an optimal solution for a floorplan **(Chen, page 470, Section 4.3 "Finding a Local Minimum", Algorithm 1 and Lemma 3).**

As per claim 2, the combination of Young and Chen already discloses a method as defined in claim 1, further comprising the step of: preparing initial data regarding panel dimension range, minimum and maximum array length and minimum and maximum array width **(Young, page 690, Section C, Algorithm Solve-LDP).**

As per claim 3, the combination of Young and Chen already discloses a method as defined in claim 2, wherein the initial data is used to limit the amount of iterations that are performed by the panel dimension loop, the array length loop and the array width loop **(Young, page 690, Section B, Algorithm Find-Width).**

As per claim 5, the combination of Young and Chen is directed to a method as defined in claim 1, wherein for each iteration of the panel dimension loop as many arrays are fitted onto the panel as possible **(Young, page 688, Section II).**

As per claim 9, the combination of Young and Chen is directed to a method as defined in claim 2, but fails to explicitly disclose wherein the step of preparing the initial data comprises inputting data using a web based graphical user interface. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a web-based GUI to input initial data in order to increase accessibility to the floorplan method.

4. **Claims 4, 6-8, and 10-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al. ("Handling Soft Modules in General Nonslicing Floorplan Using Lagrangian Relaxation") and Chen et al. ("Floorplan Sizing by Linear Programming Approximation") **in view of Murakawa (U.S. Patent No. 6,295,633 B1).**

As per claim 4, the combination of Young and Chen is directed to a method as defined in claim 2 but fails to explicitly disclose wherein the step of preparing the initial data further comprises preparing initial data on PCB and array spacing requirements, array and panel border requirements and PCB outlines. Murakawa teaches preparing initial data of on PCB and array spacing, border and outline requirements **(column 8, lines 30-36)**. Young, Chen, and Murakawa are all analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young and Chen with the spacing and border requirements of Murakawa in order to arrange physical blocks efficiently and eliminate the problem of signal delays with certainty while satisfying an increase in density of circuitry **(Murakawa, column 3, lines 11-15)**.

As per claim 6, the combination of Young and Chen is directed to a method as defined in claim 1, but fails to explicitly disclose further comprising the step of: applying array spacing and panel border specification requirements. Murakawa teaches applying spacing and border requirements **(column 8, lines 30-36)**. Young, Chen, and Murakawa are all analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young and Chen with the spacing and border requirements of Murakawa in order to arrange physical blocks efficiently and eliminate the problem of signal delays with certainty while satisfying an increase in density of circuitry **(Murakawa, column 3, lines 11-15)**.

As per claim 7, the combination of Young, Chen, Murakawa already discloses a method as defined in claim 6, further comprising the steps of: comparing the panel efficiency factors for each iteration; and selecting the highest panel efficiency factor and using its corresponding panel dimension and array size for the panel layout **(Chen, page 470, Section 4.4)**.

As per claim 8, the combination of Young, Chen, Murakawa already discloses a method as defined in claim 7, further comprising the step of: performing a sensitivity analysis in which outputs can be provided regarding possible changes to any one or more of the panel dimensions, array size, array spacing and panel border specification requirements **(Chen, page 470, "we compute the cost function change...")**.

As per claim 10, the combination of Young and Chen is directed to a method as defined in claim 9, but fails to explicitly disclose wherein the step of preparing the initial data further comprises importing an outline file of a PCB that is to be fitted into the arrays and panel. Murakawa teaches storing design data for subcircuits **(column 7, lines 60-67)** which can be PCBs **(column 18, lines 55-63)** and is functionally equivalent to importing an outline file of a PCB. Young, Chen, and Murakawa are all analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young and Chen with the outline data of Murakawa in order to arrange physical blocks efficiently and eliminate the problem of signal delays with certainty while satisfying an increase in density of circuitry **(Murakawa, column 3, lines 11-15)**.

As per claim 11, the combination of Young, Chen, Murakawa already discloses a method as defined in claim 10, wherein the outline file of the PCB provides information on a complex polygon that defines the PCB that is to be fitted into the arrays **(Murakawa, column 18, lines 12-18)**.

As per claim 12, Young is directed to a method for optimizing the fitting of Printed Circuit Boards (PCBs) onto at least one array and the at least one array onto a PCB panel, the method comprises the step of performing multiple iterations regarding different potential dimensions for the panel and the at least one array **(page 690, Section C, Algorithm Solve-LDP)** but fails to disclose determining a Panel Efficiency Factor (PEF) for each iteration *and generating optimum array and panel dimensions as well as PCB placement orientation utilizing the PEF.*

Chen teaches calculating a cost function **(page 470, Section 4.2 "Cost Function Approximation")** and *generating optimum array and panel dimensions as well as PCB placement orientation utilizing the PEF* **(Chen, page 469, Section 3.1, "Area Constraint Approximation" and Section 4, "Finding the Optimum Solution")**. Young and Chen are analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young with the efficiency factor calculation method of Chen in order to find an optimal solution for a floorplan **(page 470, Section 4.3 "Finding a Local Minimum", Algorithm 1 and Lemma 3)**.

The combination of Young and Chen fail to explicitly disclose the step of loading information regarding the outline of the PCBs *and fitting the PCBs onto the at least one array and the at least one array onto the PCB panel utilizing the optimum array and panel dimensions and PCB placement orientation*. Murakawa teaches the step of loading information regarding the outline of the PCBs **(column 7, lines 60-67)** *and fitting the PCBs onto the at least one array and the at least one array onto the PCB panel utilizing the optimum array and panel dimensions and PCB placement orientation*

(column 18, lines 51-63). Young, Chen, and Murakawa are all analogous art because they are from the same field of endeavor, floorplan sizing. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the floorplan sizing method of Young and Chen with the outline data of Murakawa in order to arrange physical blocks efficiently and eliminate the problem of signal delays with certainty while satisfying an increase in density of circuitry **(Murakawa, column 3, lines 11-15)**.

As per claim 13, the combination of Young, Chen, and Murakawa already discloses a method as defined in claim 12, wherein the information regarding the outline of the PCBs is automatically imported from a design file which provides information on a complex polygon that defines the PCB outline **(Murakawa, column 18, lines 12-18)**.

As per claim 14, the combination of Young, Chen, and Murakawa already discloses a method as defined in claim 12, further comprising the steps of: inputting information regarding panel dimensions that can be used and the minimum and maximum array length and width that can be used; and using the information inputted to determine the array and panel dimensions **(Young, page 690, Section C, Algorithm Solve-LDP)**.

As per claim 15, the combination of Young, Chen, and Murakawa already discloses a method as defined in claim 14, wherein in the inputting step, information regarding PCB and array spacing requirements and array and panel border requirements are also inputted and used to determine the array and panel dimensions **(Murakawa, column 8, lines 30-36)**.

As per claim 16, the combination of Young, Chen, and Murakawa is directed to a method as defined in claim 15, wherein in the inputting step, information regarding whether the PCBs can be rotated in the at least one array during the fitting of the PCBs onto the at least one array is entered. Young discloses obtaining information regarding whether or not the modules of the floorplan or soft or hard modules **(pages 687-688, Section II, 1st paragraph)**. Soft blocks do not have fixed parameters and allow for their height and width parameters to have floorplan functionally equivalent to that of an original module rotated.

As per claim 17, the combination of Young, Chen, and Murakawa already discloses a method as defined in claim 12, wherein the array and panel dimensions are determined by selecting the array and panel dimension combination that provides for the highest PEF **(Chen, page 470, Section 4.4)**.

As per claim 18, the combination of Young, Chen, and Murakawa already discloses a method as defined in claim 17, but fails to explicitly disclose wherein the method is performed using a web based software tool that includes a graphical user interface. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a web-based GUI to input initial data in order to increase accessibility to the floorplan method.

As per claim 19, the combination of Young, Chen, and Murakawa is directed to a method as defined in claim 17, wherein if more than one array and panel dimensions yields the highest PEF, the one having the largest array size is selected as the panelization solution. Young teaches necessity of minimizing total packing area and interconnect cost **(page 688, 3rd paragraph)**. Once the total packing area is minimized by maximizing the PEF, only way to minimize interconnect cost is to minimize the length of connections between blocks, which means maximizing block size. It would have been obvious to one of ordinary skill in the art at the time of the invention to selected the largest array size as the panelization solution given equal PEFs in order to minimize interconnect costs.

Response to Arguments

5. Applicant's arguments filed 01/05/07 have been fully considered but they are not persuasive.

6. The 35 U.S.C. 101 rejections are maintained. Even in amended form, claims 1-19 fails to produce a tangible output. In claim 1 the final result of the method of performing PCB panel optimization is "adjusting an array layout and selecting an optimum panel dimension". Given the broadest reasonable

interpretation, the final result of the method is not in a tangible form. The "adjustment" of an array layout may only be a modification of an array layout model as the specification of the instant application gives no indication that an actual physical array layout is adjusted. Additionally, the "selection" of the optimum panel dimension does not require a real world result but rather, only a logic process that exists in the abstract. Similarly, the "fitting the PCBS onto the at least one array" of claim 12 may only be a modification of a PCB panel model as the specification gives no indication that actual physical PCBs are fitted into a PCB panel.

7. In response to Applicant's remarks of the 103 rejections of claims 1 and 12, Applicant's arguments are unpersuasive because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Furthermore, in regards to claim 1, the adjusting an array layout and selecting an optimum panel dimension for the PCB panel based on optimum calculated panel efficiency is fully anticipated in using area constraints **(Chen, page 469, Section 3.1)** to find the optimum solution for circuit block placements **(Chen, page 469, Section 4)**.

Additionally, in regards to claim 12, generating optimum array and panel dimensions as well as PCB placement orientation utilizing the PEF is fully anticipated in **Chen (page 469, Section 3.1, "Area Constraint Approximation" and Section 4, "Finding the Optimum Solution")** and fitting PCBs onto one array and array onto the PCB panel using optimum dimensions and placement orientations **(Murakawa, column 18, lines 51-63)**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

1. "A New Method for Floor Planning Using Topological Constraint Reduction" published by Vijayan et al. in 1991.

2. "VLSI Cell Placement Techniques" published by Shahookar et al. in June 1991.

3. "Combine and Top Down Block Placement Algorithm for Hierarchical Logic VLSI Layout" published by Kozawa et al. in 1984.

4. U.S. Patent No. 5,682,322 issued to Boyle et al. on 10/28/97.

5. U.S. Patent No. 6,742,165 B2 issued to Lev et al. on 05/25/04.

6. U.S. Patent No. 5,898,597 issued to Scepanovic et al. on 04/27/99.

7. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
03/19/07

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SUPERVISORY PATENT EXAMINER